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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BUR920030168US1

In Re Application Of: **Anand et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/707071	11/19/03		024241	2186	1070

Title: **AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS.**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS.

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.

- ☒ Charge the amount of
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.

Certificate of Transmission by Facsimile*

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Signature of Person Mailing Correspondence

Phyllis deLangis

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Robert A. Walsh

Signature

Dated: 8/17/2004

Robert A Walsh, Esq.
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IBM Microelectronics
1000 River Street - 972E
Essex Junction, VT 05452

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Darren L. Anand, et al

Examiner: Unassigned

Serial No.: 10/707071

Group Art Unit: 2186

Filed: 11/19/03

Docket: BUR920030168US1 (17124)

For: AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS

Dated: 8-17-04

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

Applicants are submitting a copies of the cited references, along with English language abstracts. The relevance of the above-identified reference has been described in the specification.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

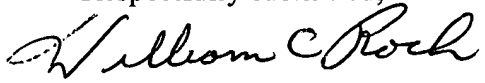
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450 on 8/18/04.

Dated: 8/18/04

B. de Sanges

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,



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INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920030168 (17124)	10/707071
Applicant(s)	
Darren L. Anand, et al.	
Filing Date	**Group Art Unit**
11-19-03	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		JP7078495	20/3/95	Japan				
		JP2002243801	28/08/02	Japan				
		JP2002298598A	11/10/02	Japan				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		International Test Conference, 1998 Proceedings, "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories", Ivo Schanstra, Dharmajaya Lukita, Ad J. van de Goor, Kees Veelenturf, Paul J. van Winjnen, pp. 872-881

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.